Remarks/Arguments

The Final Office Action dated March 29, 2005, has been received and carefully reviewed.

Claims 2, 3, 13, 14 and 20 are objected to for depending on a rejected base claim. Claims 8, 25 and 26 stand rejected under 35 U.S.C. §112, second paragraph. Claims 8, 25 and 26 have been amended to overcome this rejection. Claim 27 has been indicated to be allowable. Claim 25 has been indicated to be allowable if corrected to overcome the 35 U.S.C. §112, second paragraph rejection.

Claims 1, 4, 6, 7, 9 - 11, 15, 18, 19, 21 and 22 stand rejected under 35 U.S.C. § 102 (e) as being anticipated by Bunting et al. (U.S. 5,796,743, hereinafter "Bunting"). Claims 5, 16 and 17 stand rejected under 35 U.S.C. § 103 (a) as applied to claims 1, 4, 6, 7, 9 - 11, 15, 18, 19, 21 and 22 and in further view of Takayama (U.S. 5,991,842 A, hereinafter "Takayama"). Claims 12 and 23 stand rejected under 35 U.S.C. § 103 (a) as applied to claims 1, 4, 6, 7, 9 - 11, 15, 18, 19, 21 and 22 and in further view of Sato et al. (U.S. 6,259,694 B1, hereinafter "Sato"). The rejections are respectfully traversed.

Independent Claim 1, as amended, recites:

> A method for assembling data packets for isochronous data transmission via a data bus, a data format for the isochronous data transmission being defined in an isochronous data format header of a bus packet, comprising the steps of:
>
> writing the isochronous data format header to a special register and to a buffer memory for the data packets when the isochronous data transmission is set up in a data transmitting device;
>
> attaching useful data of the data packet to the isochronous data format header in the buffer memory; and
>
> taking both the isochronous data format header and the useful data from said buffer memory for data transmission. (emphasis added)

The present invention is directed to a method and apparatus for assembling data packets for isochronous data transmission via a data bus. In particular, the present invention simplifies the method and circuitry for the preparation and processing of the data packets by reducing the circuitry and simplifying the method. This is accomplished by omitting as much as possible the selection logic unit (e.g., multiplexer) "for joining

together the CIP header and the associated useful data". This is further accomplished by writing the "generated CIP header ... to the buffer memory for the useful data, in which case the useful data of the data packet are subsequently attached to this CIP header in the buffer memory (see Claim 1). What is achieved as a result of this is that, for the transmission of the data via the bus, the data transmitting section only has to access the buffer memory for the useful data, where CIP header and useful data are stored contiguously in the correct order. The data transmitting section thus obtains the data to be transmitted only via the buffer memory. A selection logic unit which determines the special register from which the CIP header has to be taken and the memory area of the buffer area from which the useful data have to be attached can be omitted." (see page 3, line 32 to page 4, line 8).

It should further be noted that since an inventor can be his own lexicographer, the inventors have defined "isochronous" with respect to the present application at page 1, line 37 to page 2, line 1, as " that data to be transmitted arise regularly at a data source, the data also arising with approximately the same size each time." In particular, the present application nowhere discusses the use of a clock signal or any delay.

Bunting describes joining data with a packet alignment flag (PAF) using a data/header combiner circuit 15, which includes a data FIFO 16 and a header FIFO 17 as depicted in Fig. 1 and more particularly in Fig. 17, which includes details of data/header combiner 15. It can be clearly seen from Fig. 17 and col. 8, lines 9 - 39 that the data/header combiner 15 of Bunting includes separate data and header FIFOs (72 and 70 respectively) and a multiplexer 76 (e.g., selection logic unit). Very specifically, at page 4, lines 7 - 17, Bunting describes the use of a signal delay network, which among other things insures proper time synchronism. The Examiner has indicated that is "anticipates that said data packets are for isochronous data transmission". Applicants fail to recognize that the above description in Bunting anticipate isochronous data transmission as defined by the inventors for the present invention given that the present invention does not use a clock signal or any form of delay. Further, Bunting requires a PAF "to ascertain the completion of 32-bit data words, assembled from a stream of

variable length codewords, and the completion of 960-bit long data packets." See page 3, lines 30 - 34.

Further, the Examiner points to buffer memory including Header FIFO 70, Data FIFO 72 and Rate buffers 713 and 714. Since neither Header FIFO 70 nor Data FIFO 72 store both parts of a data packet (header and data), only Rate buffer 713 and 714 correspond to the buffer of the present invention. Header FIFO 70 and Data FIFO 72 do not read on claim 1 because as recited in claim 1 there is a " taking both the isochronous data format header and the useful data from said buffer memory for data transmission" that does not occur in Bunting. Claim 1 of the present invention further recites "writing the isochronous data format header to a special register and to a buffer memory for the data packets when the isochronous data transmission is set up in a data transmitting device". According to Bunting's Fig. 17 the Rate Buffers 713, 714 are located behind the Output Register 78. Ahead of the Output Register a Header/Data Multiplexer 76 is positioned that fetches header data from Header FIFO 70 and data from Data FIFO 72. The design of Data and Header Combiner 15 shows that during set up of a data transmission the header data is written into the Header FIFO 70 only. That is, there is no bus connection between Header Generator 18 and Output Register 78 or Rate Buffers 713 and 714. See also page 14, lines 19 to 29 of Bunting. Therefore, writing of the header to the special register and to the buffer memory during set up of an isochronous data transmission does not occur. Further, the Output Register 78 of Bunting, while denominated "register", is in fact not a register. On page 16, lines 6-9 it is explained that component 78 is an Output Buffer in which storage capacity for more than a complete packet is available.

It is respectfully submitted that, in fact, Bunting teaches away from the present invention. As recited in independent claim 1, the present invention is directed to isochronous data transmission as defined in the application and both the isochronous data format header and the payload (useful data) are taken from a buffer in which the packet is already formed in the correct format. For at least the reasons stated above, it is further respectfully submitted that the present invention is, therefore, not anticipated and is patentable over Bunting.

Independent claims 6, 9 and 18 have features similar to those recited in claim 1. Specifically, while claims 9 and 18 do not recite isochronous data transmission, they do recite the use of a register and a buffer memory, which are distinquishable over those described in Bunting as explained above. It is, therefore submitted that claims 6, 9 and 18 are also not anticipated and patentable over the art of record.

Regarding claims 5, 16 and 17, Takiyama describes the format of a CIP packet and that a source packet may be divided in a number of data blocks, but is silent to how the CIP packet is formed in memory. In particular, Takiyama does not describe the use of a single buffer (or FIFO) for assembling data or simplification of the method and circuitry required for assembling data packets by omitting a selection logic unit from the combiner circuitry.

Regarding claims 12 and 23, Sato describes in detail the isochronous cycle of a IEEE 1394 bus inclusive of the isochronous bus packet format and the late check (error bit). Sato also describes at col. 10, line 35 to 40 that the post-transmission circuit 107 adds the 1394 header and CIP header to the data containing a source packet header stored in the FIFO. Data flow in Fig. 5 is from FIFO 110 to Link Core 101 via post processing unit 107. The CIP header is added to the source packet 'On the Fly'. This teaches away from the present invention in which both the CIP header and the source packet data is taken/read from the buffer memory.

It is respectfully submitted that Bunting alone or in combination with either Takiyama or Sato does not include all of the features of the present invention. In light of the above remarks, it is respectfully submitted that independent claims 1, 6, 9, and 18, for at least the reasons stated above, are unanticipated and patentable over the art of record. Claims 2 - 5 depend directly or indirectly from claim 1. Claims 7 - 8 depend directly from claim 6. Claims 10 - 17 depend directly or indirectly from claim 9. Claims 19 - 23 depend directly from claim 18. It is, therefore, respectfully submitted that claims 2 - 5, 7 - 8, 10 - 17 and 19 - 23 are also unanticipated and patentable for at least the reasons discussed above as well as the additional features recited therein.

Independent claims 25 and 27 have been indicated to be allowable. Independent claim 24 recites features similar to those recited in independent claim 1 and is believed

to be not anticipated and patentable over the art of record for at least the reasons given above. Independent claim 26 does not recite isochronous data transmission, but does recite the use of a register and a buffer memory, which are distinquishable over those described in Bunting as explained above. It is, therefore, respectfully submitted that independent claim 24 and 26 are also unanticipated and patentable over the art of record.

If you have any questions regarding this response, please do not hesitate to contact me.

However, should it be determined that any further charges are associated with this response, please charge any costs that may be associated with the filing of this response, to Deposit Account No. 07-0832.

Respectfully submitted,
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